CLAIMS

What is claimed is:

1. A method, comprising:

loading a local memory resource for a processor core of NUMA design with a functional test program, the processor core being able to access non-local memory resources through a link control mechanism;

providing an external path for test signals generated by the processor core during execution of the functional test program.

2. The method of claim 1, wherein the external path loops the test signals from the link control mechanism back to the link control mechanism.

3. The method of claim 2, wherein the link control mechanism comprises first and second link controllers and the external paths bridge the test signal between the first and second link controllers.

4. The method of claim 3, further comprising providing a response agent that is capable of responding to the test signal.

5. The method of claim 1, wherein the external path is provided by an automatic test equipment.

6. The method of claim 5, wherein the loading is performed using the automatic test equipment.

7. The method of claim 1, wherein the local memory resource comprises cache memory.

8. The method of claim 7, further comprising enabling the processor core to operate in a test mode wherein the processor core executes a boot program directly from the cache memory.

9. A method, comprising:

generating a test signal in a first unit of a semiconductor die;

sending the test signal to a second unit of the semiconductor die via a high speed interconnect;

receiving a response to the test signal from the second unit, wherein the test signal and the response is routed through an external off-chip loop that bridges first and second input/output interfaces of the high speed interconnect.

10. The method of claim 9, wherein the test signal comprises a data request.

11. The method of claim 10, wherein the test signal comprises an instruction request.

12. The method of claim 9, wherein the first unit comprises a first processor, and the second unit comprises a second processor.

13. The method of claim 9, wherein the first and second high speed input/output interfaces comprise high speed links.

14. The method of claim 13, wherein the external off-chip loop is provided by an automatic test equipment.

15. The method of claim 9, wherein the test signal is generated using a test program stored in a cache for the first unit.

16. The method of claim 9, further comprising generating a response in a response agent.

17. The method of claim 16, wherein sending the test signal to the second unit comprises determining an address for the response agent using a switching mechanism.

18. The method of claim 17, wherein the switching mechanism includes a crossbar switch mechanism.

19. The method of claim 9, further comprising analyzing the response.

20. The method of claim 9, further comprising storing the response in cache memory for subsequent downloading to an automatic test equipment for analysis.

21. A system, comprising:

first and second processing units;

first and second link interfaces associated with each of the first and second processing units, respectively;

a cache memory associated with the first processing unit, the cache memory storing a test program therein to generate a test signal;

a switching mechanism to switch the test signal to the second processing unit via an external path that bridges the first and second link interfaces; and

a response agent associated with the second processing unit to generate a response to the test signal.

22. The system of claim 21, wherein in a test mode, the system is configured to boot off the cache memory.

23. A method, comprising:

loading a memory within a link-based system with a functional test program;

executing the functional test program in a processor core of the link-based system; and

routing test signals generated during execution of the functional test program to a response agent embedded in the link-based system via an external path.

24. The method of claim 23, wherein the external path is defined by a test interface board.